FIG. 1
(Prior Art)

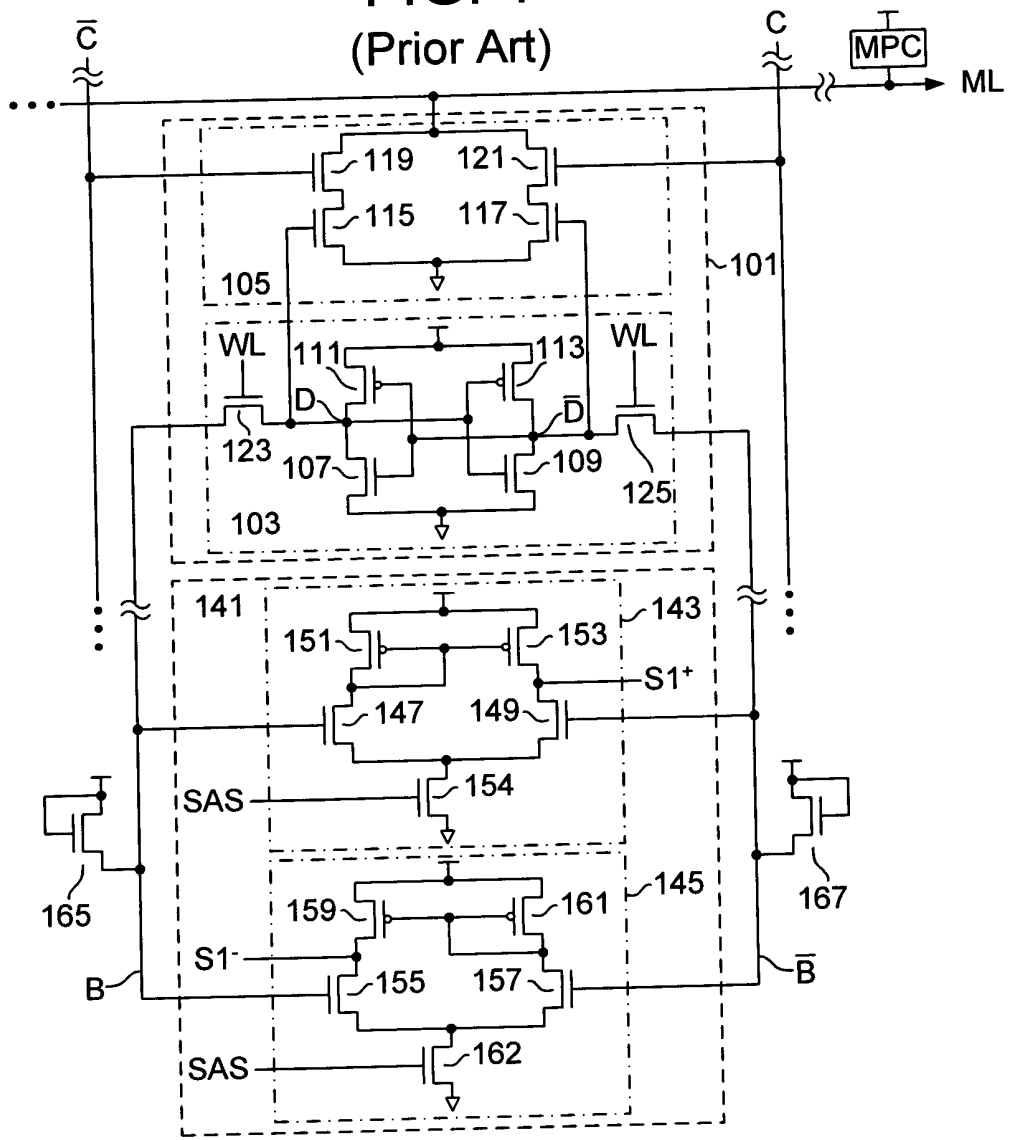


FIG. 2
(Prior Art)

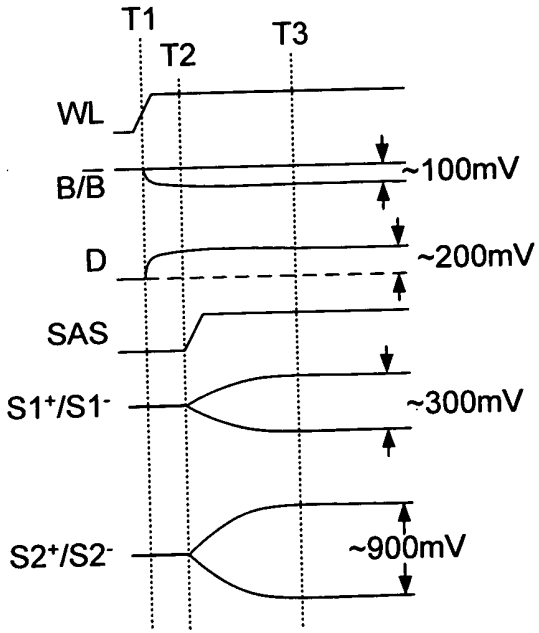


FIG. 3

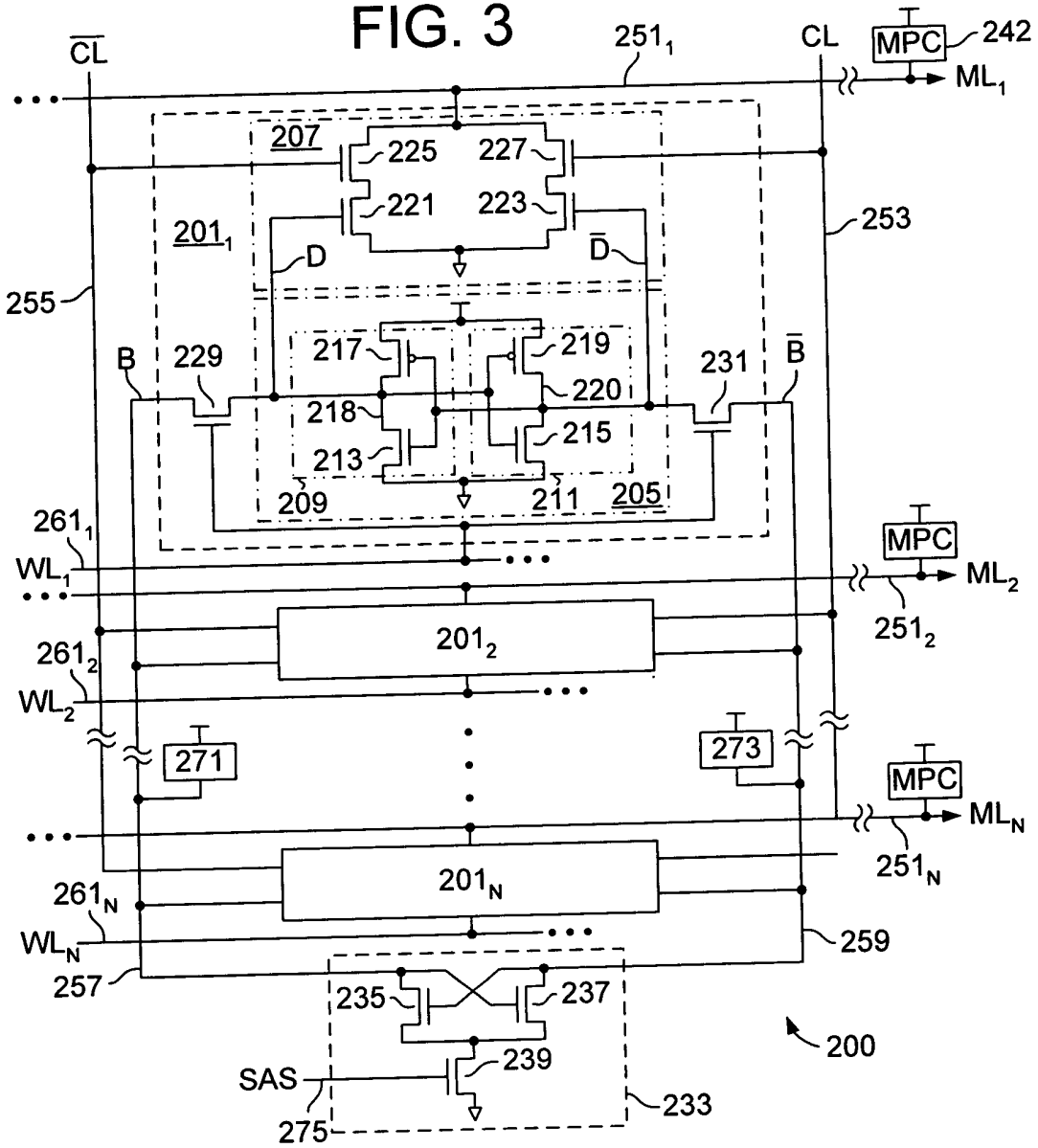
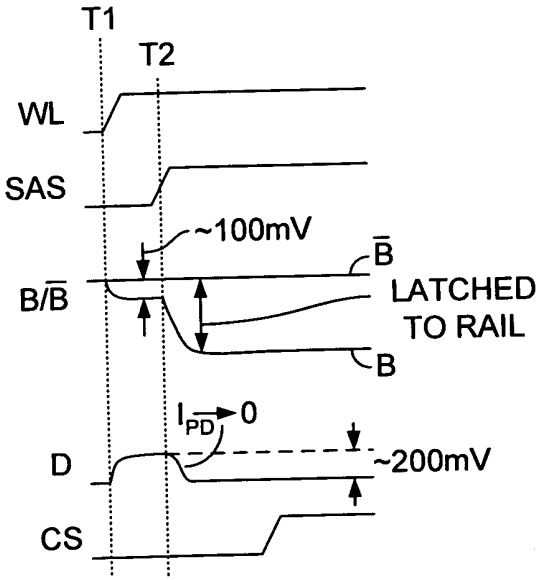

CL
251_1
CL
MPC
242
ML_1
207
225
227
221
223
201_1
D
D
253
255
B
229
217
219
220
231
B
218
215
213
209
211
205
261_1
WL_1
MPC
ML_2
251_2
201_2
261_2
WL_2
271
273
MPC
ML_N
251_N
201_N
261_N
WL_N
259
257
235
237
239
SAS
233
275
200

FIG. 4


T1
T2
WL
SAS
~100mV
B
B/B
LATCHED
TO RAIL
B
I_{PD}
0
D
~200mV
CS

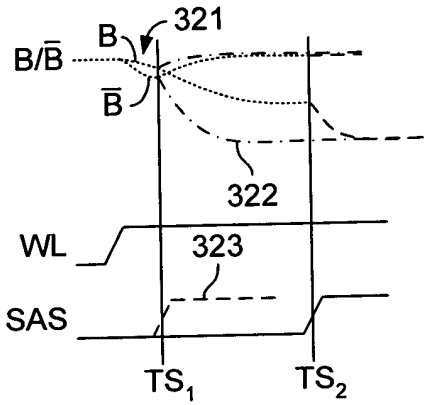


FIG. 5

FIG. 6

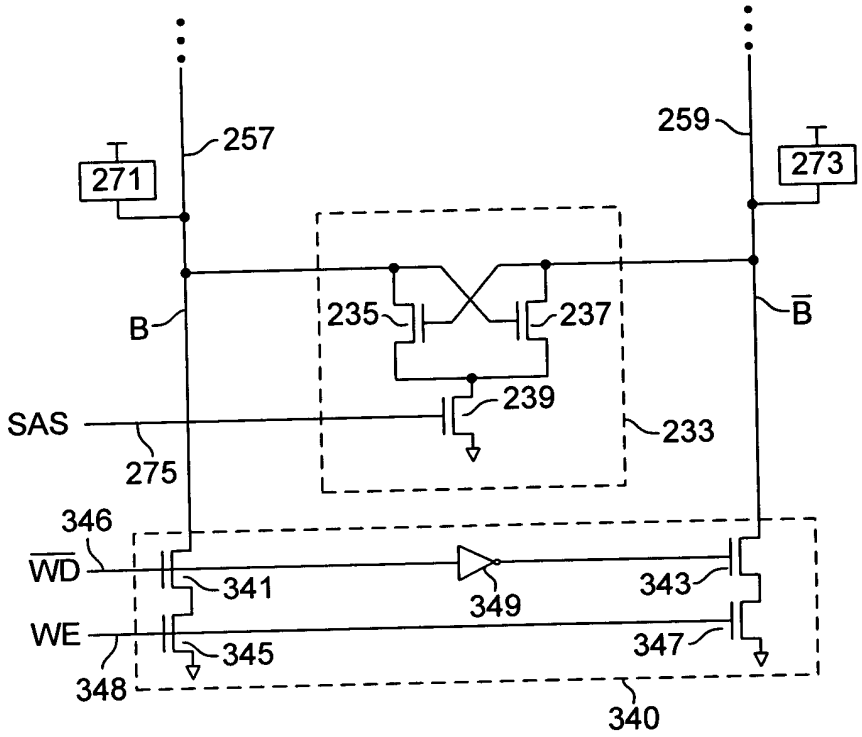


FIG. 7

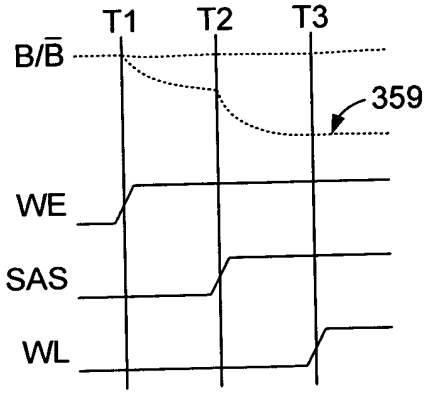


FIG. 8

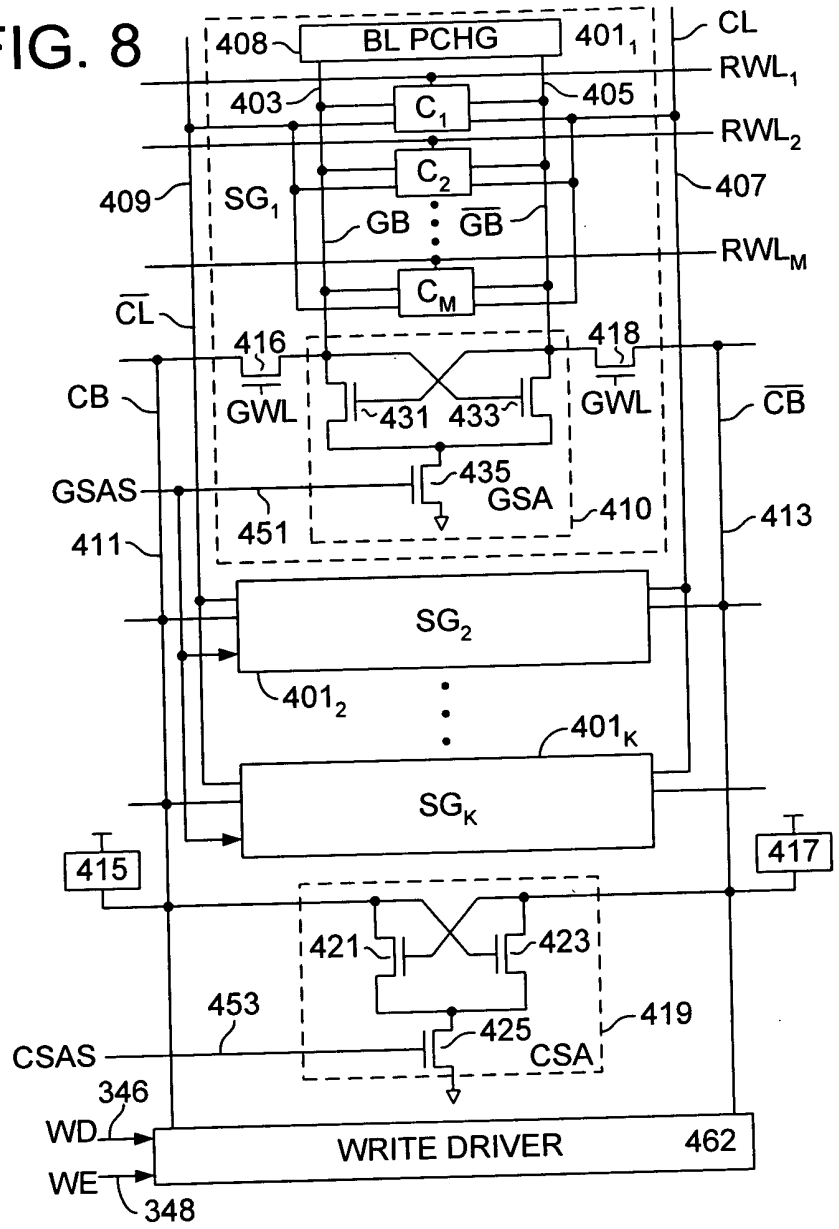


FIG. 9

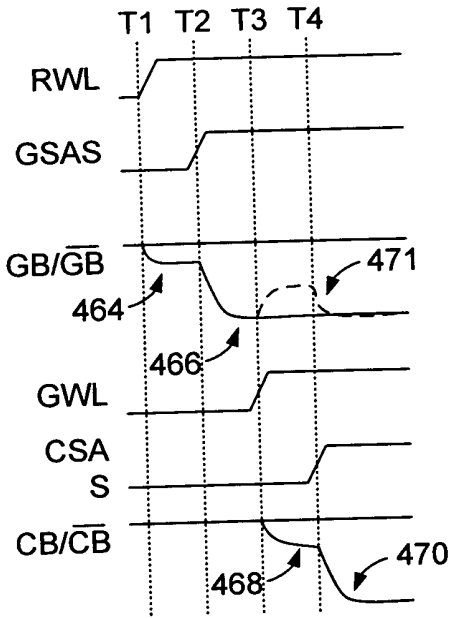
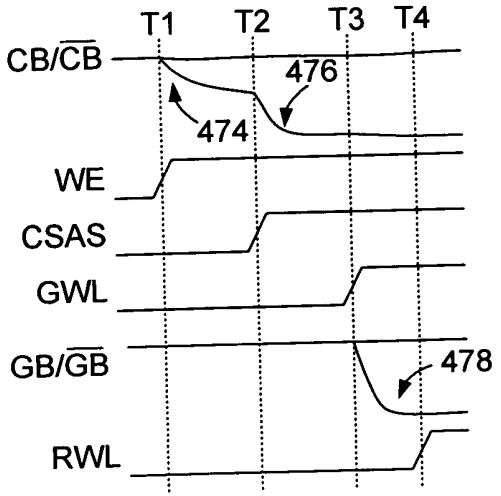


FIG. 10



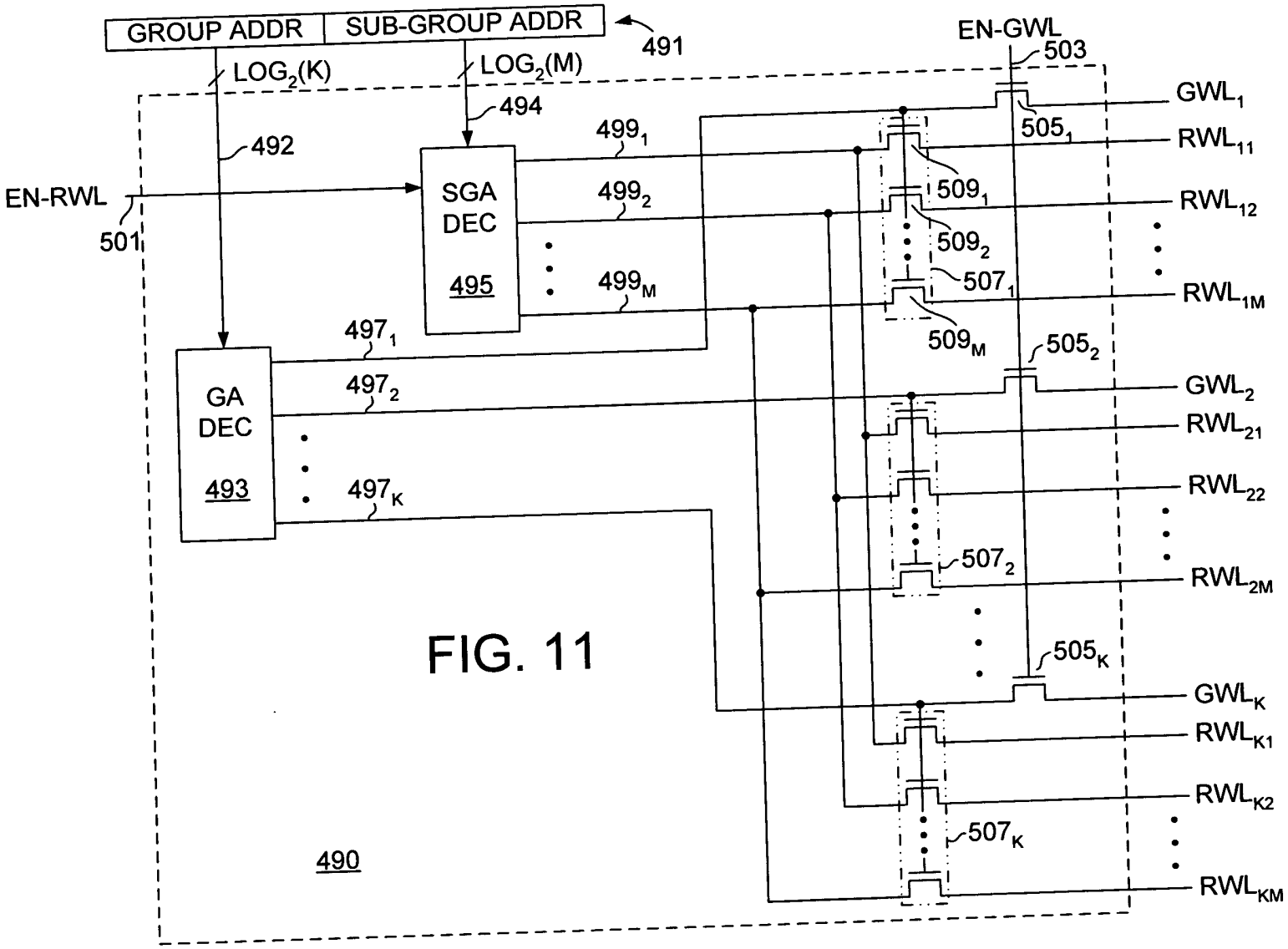

GROUP ADDR
SUB-GROUP ADDR
491
LOG2(K)
LOG2(M)
494
492
EN-RWL
501
SGA DEC
495
499_1
499_2
499_M
GA DEC
493
497_1
497_2
497_K
EN-GWL
503
505_1
505_2
505_K
509_1
509_2
509_M
507_1
507_2
507_K
GWL_1
RWL_11
RWL_12
RWL_1M
GWL_2
RWL_21
RWL_22
RWL_2M
GWL_K
RWL_K1
RWL_K2
RWL_KM
490

FIG. 11

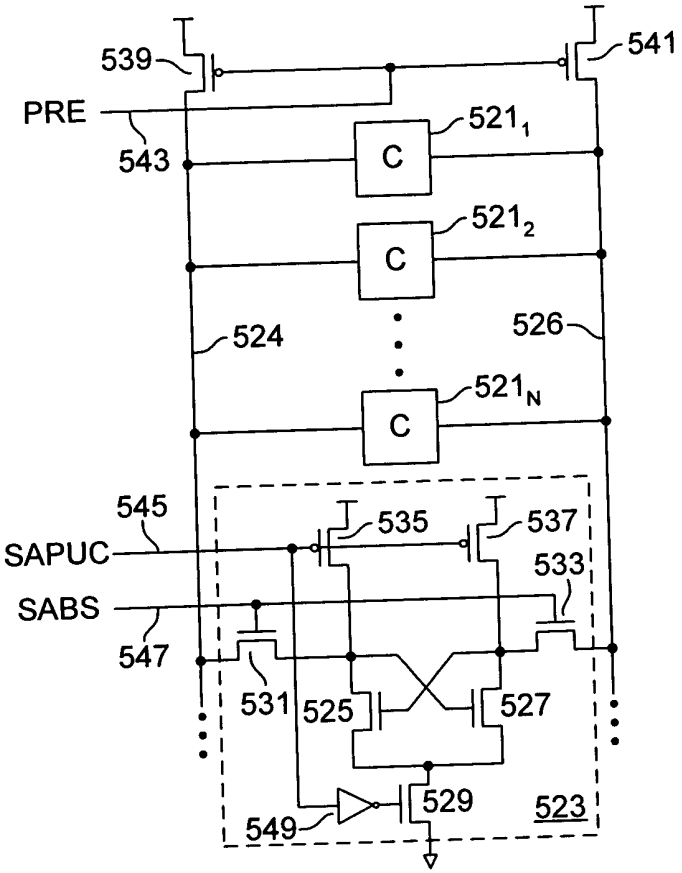

539
541
PRE
543
521_1
C
521_2
C
524
526
521_N
C
545
535
537
SAPUC
533
SABS
547
531
525
527
529
523
549

FIG. 12

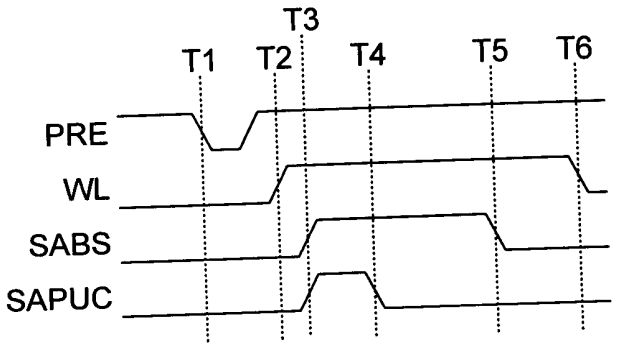

T1
T2
T3
T4
T5
T6
PRE
WL
SABS
SAPUC

FIG. 13

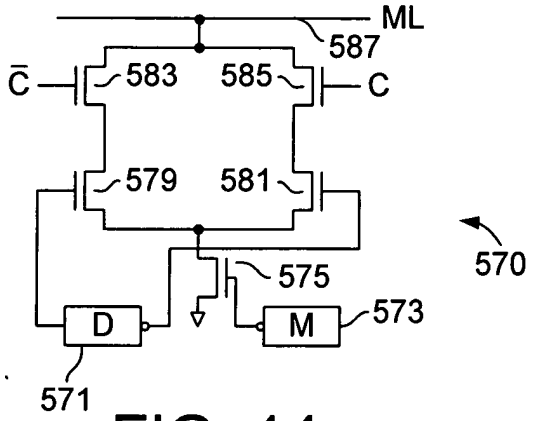


FIG. 14

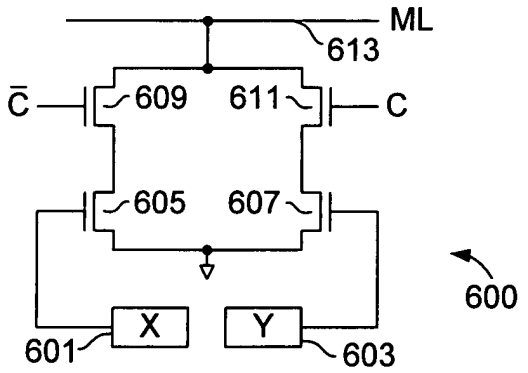
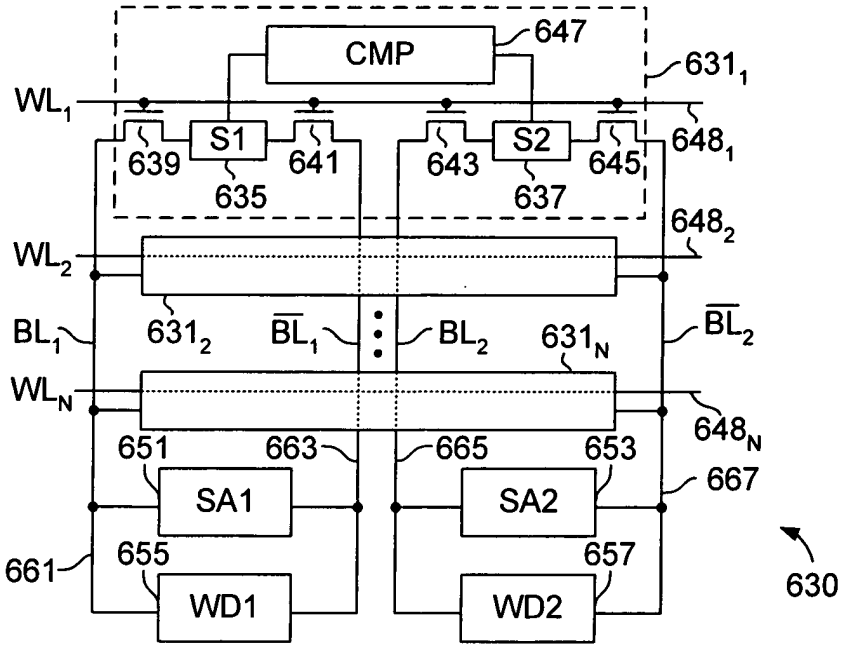


FIG. 15

FIG. 16



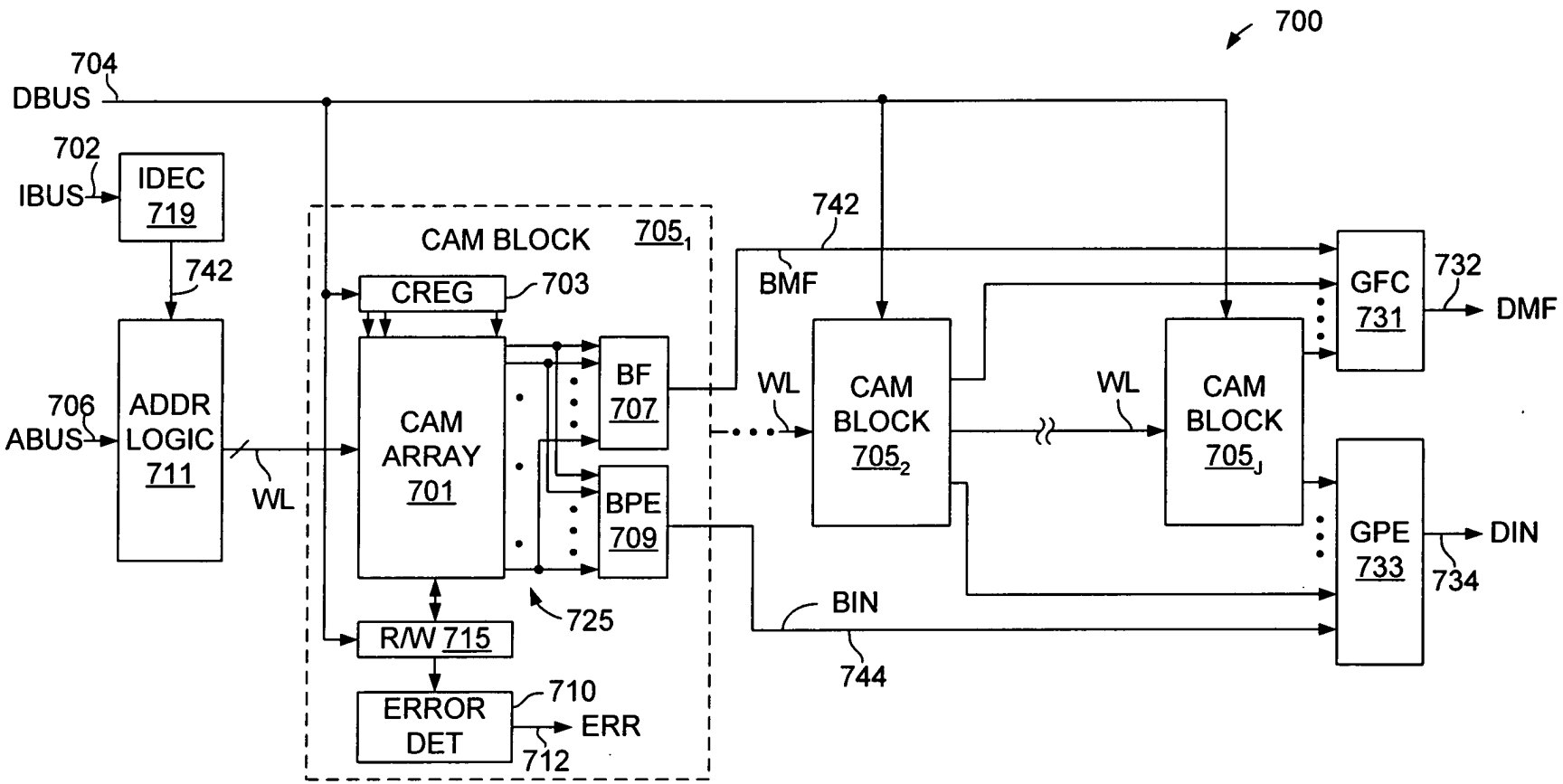

700
704
DBUS
702
IBUS
IDEC
719
742
706
ABUS
ADDR
LOGIC
711
WL
CAM BLOCK
705_1
CREG
703
CAM
ARRAY
701
BF
707
BPE
709
725
R/W 715
ERROR
DET
710
ERR
712
742
BMF
WL
CAM
BLOCK
705_2
WL
CAM
BLOCK
705_J
GFC
731
732
DMF
GPE
733
DIN
734
BIN
744

FIG. 17